



April 1995  
Revised July 2005

# 74LCX11

## Low Voltage Triple 3-Input AND Gate with 5V Tolerant Inputs

### General Description

The LCX11 is a triple 3-input AND gate with buffered outputs. LCX devices are designed for low voltage (2.5V or 3.3V) operation with the added capability of interfacing to a 5V signal environment.

The 74LCX11 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V  $V_{CC}$  specifications provided
- 6.0ns  $t_{PD}$  max ( $V_{CC}$  = 3.3V), 10  $\mu$ A  $I_{CC}$  max
- Power down high impedance inputs and outputs
- $\pm$ 24 mA output drive ( $V_{CC}$  = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds JEDEC 78 conditions
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Leadless DQFN Package

### Ordering Code:

Order Number	Package Number	Package Description
74LCX11M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX11MX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LCX11SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX11BQX (Note 2)	MLP014A	Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm
74LCX11MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LCX11MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Pb-Free package per JEDEC J-STD-020B.

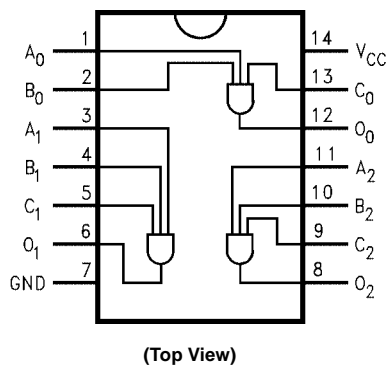
**Note 1:** "\_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

**Note 2:** DQFN package available in Tape and Reel only.

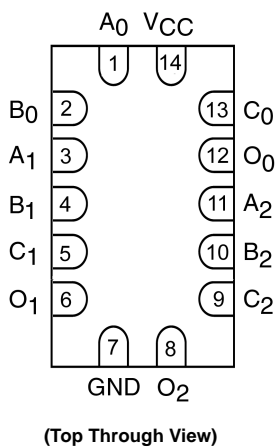
74LCX11 Low Voltage Triple 3-Input AND Gate with 5V Tolerant Inputs

## Connection Diagrams

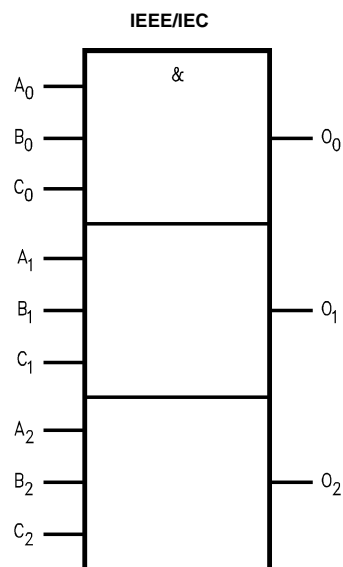
Pin Assignments for SOIC, SOP, and TSSOP



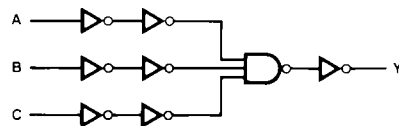
Pad Assignments for DQFN



## Logic Symbol



## Logic Diagram



## Pin Descriptions

Pin Names	Description
$A_n, B_n, C_n$	Inputs
$O_n$	Outputs

Absolute Maximum Ratings <sup>(Note 3)</sup>					
Symbol	Parameter	Value	Conditions	Units	
V <sub>CC</sub>	Supply Voltage	−0.5 to +7.0		V	
V <sub>I</sub>	DC Input Voltage	−0.5 to +7.0		V	
V <sub>O</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> + 0.5	Output in HIGH or LOW State (Note 4)	V	
I <sub>IK</sub>	DC Input Diode Current	−50	V <sub>I</sub> < GND	mA	
I <sub>OK</sub>	DC Output Diode Current	−50 +50	V <sub>O</sub> < GND V <sub>O</sub> > V <sub>CC</sub>	mA	
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA	
I <sub>CC</sub>	DC Supply Current per Supply Pin	±100		mA	
I <sub>GND</sub>	DC Ground Current per Ground Pin	±100		mA	
T <sub>STG</sub>	Storage Temperature	−65 to +150		°C	

### Recommended Operating Conditions <sup>(Note 5)</sup>

Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V <sub>I</sub>	Input Voltage	0	5.5	V	
V <sub>O</sub>	Output Voltage	HIGH or LOW State	0	V <sub>CC</sub>	V
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V – 3.6V V <sub>CC</sub> = 2.7V – 3.0V V <sub>CC</sub> = 2.3V – 2.7V		±24 ±12 ±8	mA
T <sub>A</sub>	Free-Air Operating Temperature	−40	85	°C	
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V	

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.

**Note 4:** I<sub>O</sub> Absolute Maximum Rating must be observed.

**Note 5:** Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = −40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3 – 2.7 2.7 – 3.6		0.7 0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = −100 μA I <sub>OH</sub> = −8 mA I <sub>OH</sub> = −12mA I <sub>OH</sub> = −18mA I <sub>OH</sub> = −24mA	2.3 – 3.6 2.3 2.7 3.0 3.0	V <sub>CC</sub> − 0.2 1.8 2.2 2.4 2.2		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA I <sub>OL</sub> = 8 mA I <sub>OL</sub> = 12mA I <sub>OL</sub> = 16 mA I <sub>OL</sub> = 24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0		0.2 0.6 0.4 0.4 0.55	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6V ≤ V <sub>I</sub> ≤ 5.5V	2.3 – 3.6 2.3 – 3.6		10 ±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> −0.6V	2.3 – 3.6		500	μA

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500 Ω						Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30pF		
		Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t <sub>PHL</sub>		1.5	6.0	1.5	7.0	1.5	7.2	
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew (Note 6)		1.0 1.0					ns

**Note 6:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ).

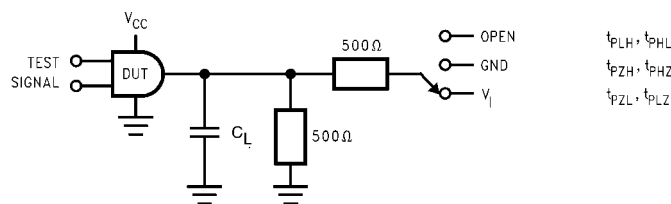
## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^{\circ}\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\ \text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$ $C_L = 30\ \text{pF}, V_{IH} = 2.5\text{V}, V_{IL} = 0\text{V}$	3.3 2.5	0.8 0.6	V
$V_{OLV}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\ \text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$ $C_L = 30\ \text{pF}, V_{IH} = 2.5\text{V}, V_{IL} = 0\text{V}$	3.3 2.5	-0.8 -0.6	V

## Capacitance

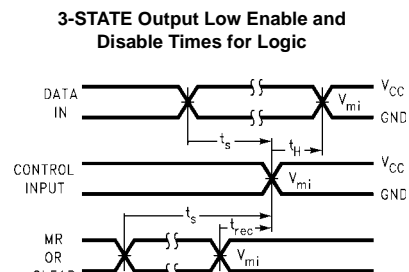
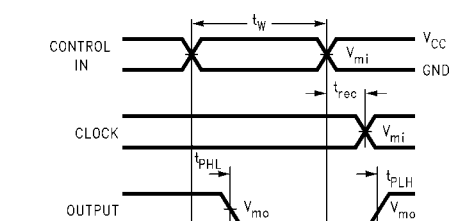
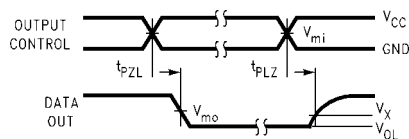
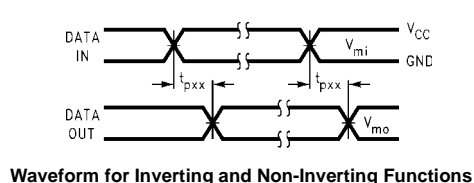
Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0\text{V or } V_{CC}$	7	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}, f = 10\ \text{MHz}$	25	pF

## AC Loading and Waveforms Generic for LCX Family

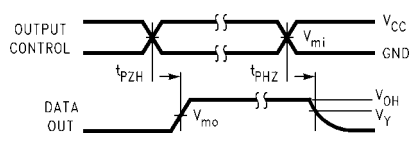


**FIGURE 1. AC Test Circuit**  
( $C_L$  includes probe and jig capacitance)

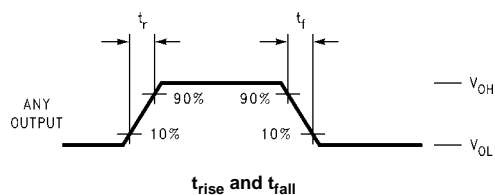
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZH}, t_{PHZ}$	GND



**Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



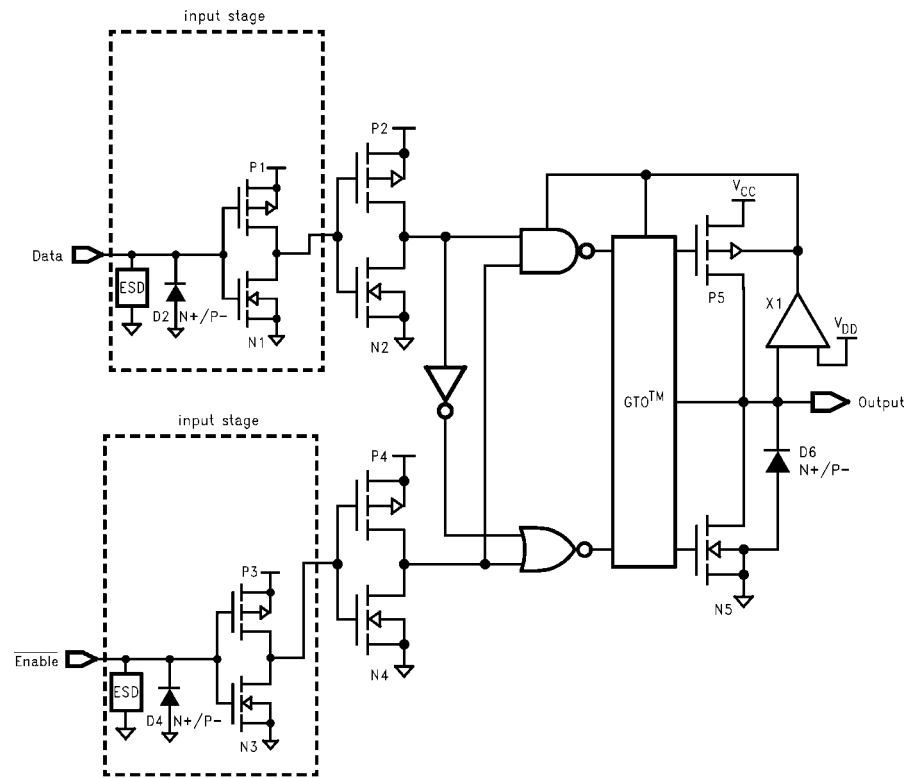
**Setup Time, Hold Time and Recovery Time for Logic**



**FIGURE 2. Waveforms**  
(Input Pulse Characteristics;  $f = 1\text{MHz}$ ,  $t_r = t_f = 3\text{ns}$ )

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

# Schematic Diagram Generic for LCX Family

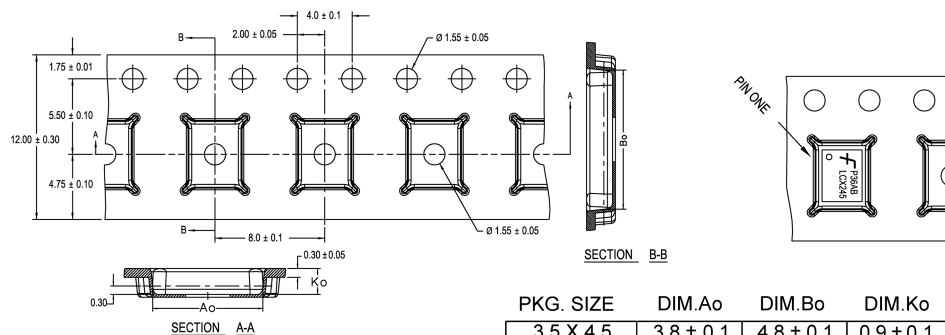


## Tape and Reel Specification

### Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### TAPE DIMENSIONS inches (millimeters)



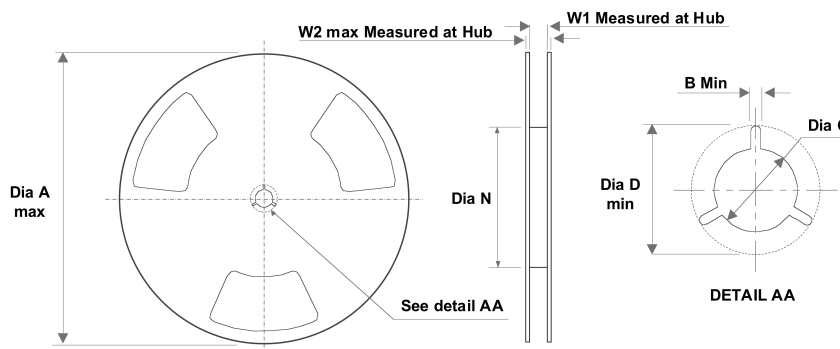
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

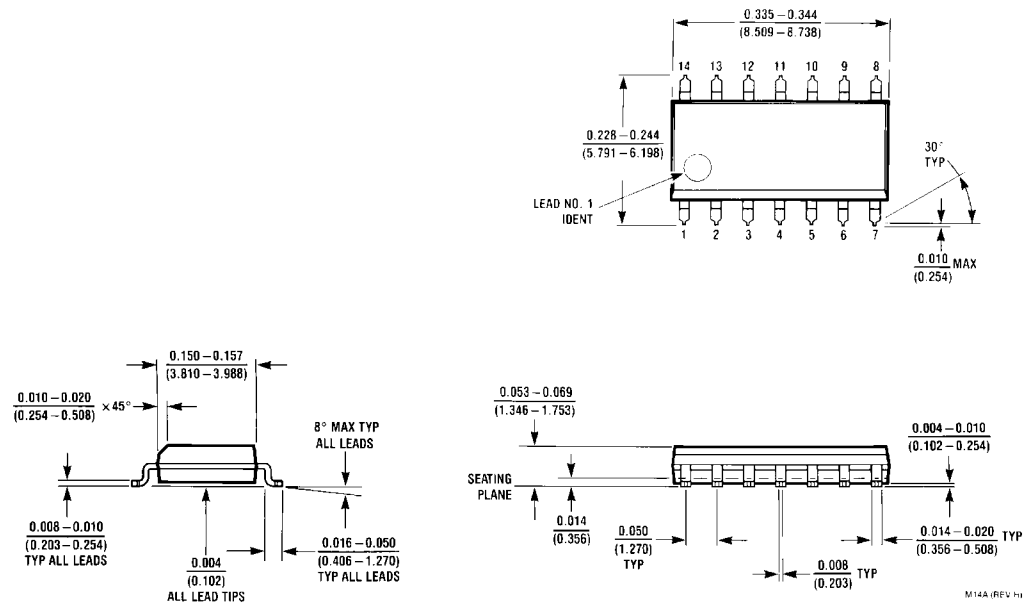
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. A<sub>o</sub> and B<sub>o</sub> measured on a plane 0.120[0.30] above the bottom of the pocket.
6. K<sub>o</sub> measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

### REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330.0)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.488 (12.4)	0.724 (18.4)

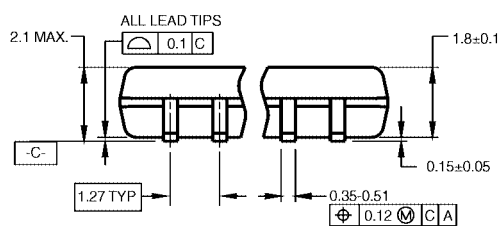
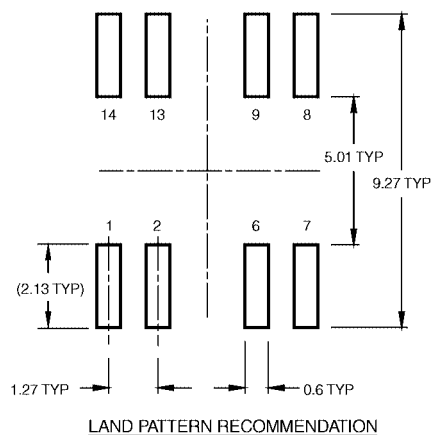
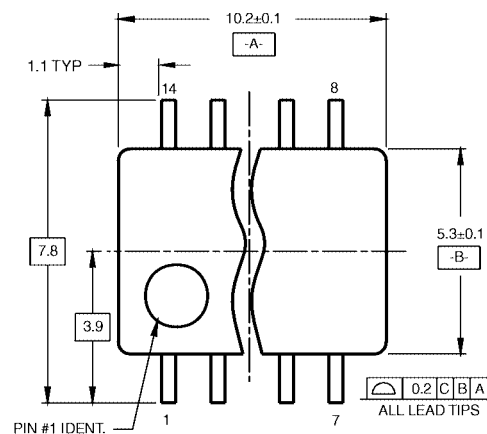
# Physical Dimensions inches (millimeters) unless otherwise noted



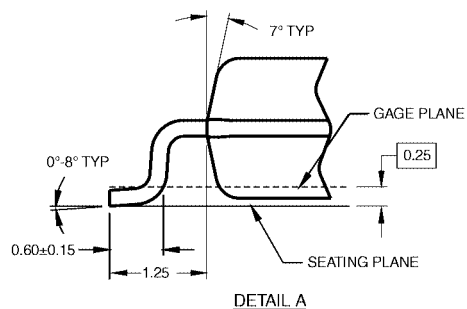
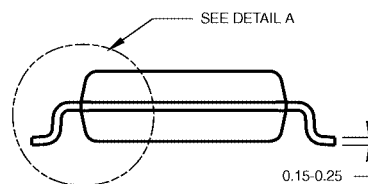
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**



# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



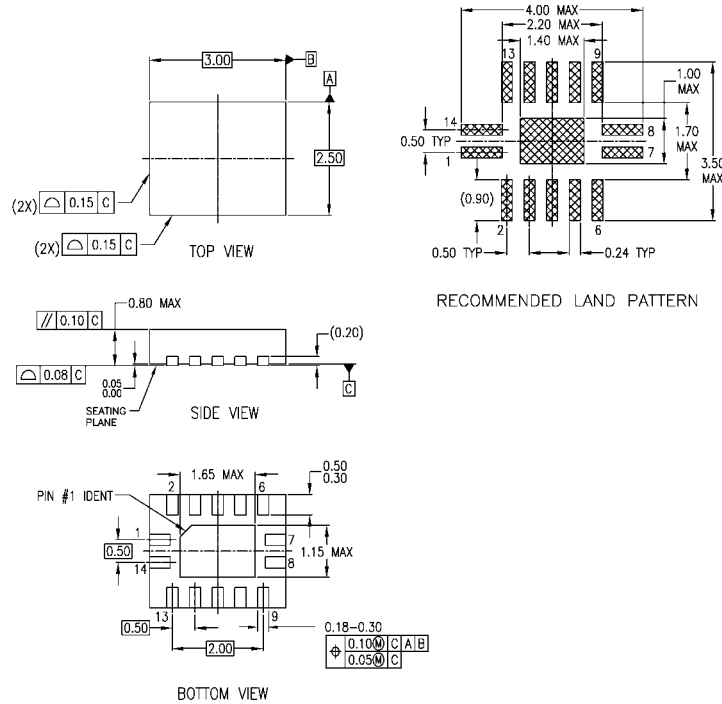
## NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M14D**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



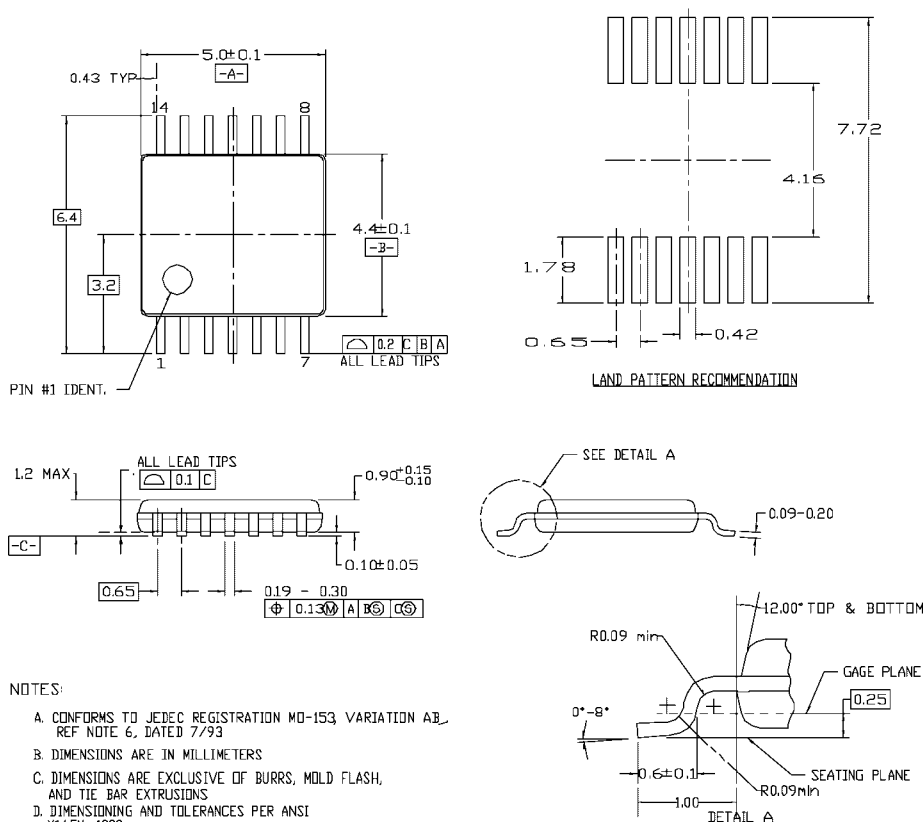
## NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP014ArevA

**Pb-Free 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0mm  
Package Number MLP014A**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC14

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